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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,491	12/31/2003	Keith D. Jones	42P17767	1802

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EXAMINER	
CLARK, SHEILA V	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 02/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,491	JONES, KEITH D.	
	Examiner	Art Unit	
	S. V. Clark	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,10,12,14 and 17-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,10,12,14 and 17-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jin et al.

Jin et al shows in figure 7 a substrate 61 formed of a build up layer comprising at least one binder (i.e. epoxy) and at least one filler having a negative coefficient of expansion embedded within. Chip 63 in figure 7 is shown and at least one interconnect 64 is shown disposed between the substrate and the die.

The term "build up" layer fails to be specifically defined in the claims fails to have a special meaning that would limit the structure of said layer. Further said term is not established to have any well known meaning in this art to define it to have a specific characteristic. Therefore the term 'build up layer" in the claims is being considered to have an obvious meaning as a "layer of material" or "material structure" in the broadest sense.

With respect to claim 4, substrate 7 is considered to have an internal structure or core comprising at least one binder (i.e. epoxy) and at least one filler having a negative coefficient of expansion

Claims 2, 3, 5, 6, 18, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jin et al in view of Starkovich and Chuang.

The features of Jin et al relative to the claims in which these claims depend have been discussed above. Though Jin et al teaches use of filler materials having a negative coefficient of expansion he fails to specifically mention use of zirconium tungstate. Substrates formed with at least one binder and at least one filler having a negative coefficient of expansion are taught by both Starkovich and Chung and where said one filler comprises zirconium tungstate. It would have therefore been obvious to one having ordinary skill in this art to use zirconium tungstate as recited in claims 2, 5, 18 and zirconium tungstate having the characteristics recited in claims 3,6, 19 in the device because the materials suggested by Jin et al are not limited to those in particular and Col. 2, lines 60-65 teach use of negative coefficient of expansion materials having the characteristics recited in claims 3, 6 which would include zirconium tungstate and used of zirconium tungstate as a filler material for the purpose of reducing the coefficient of thermal expansion of the build up layer to closely match that of the chip is also taught by Starkovich and Chuang to be well known.

Claims 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jin et al in view of Starkovich and Chuang.

Jin et al shows in figure 7 a material 7 for use as a build up dielectric layer comprising at least one binder (i.e. epoxy) and at least one filler having a negative coefficient of expansion.

The term "build up" layer fails to be specifically defined in the claims fails to have a special meaning that would limit the structure of said layer. Further said term is

not established to have any well known meaning in this art to define it to have a specific characteristic. Therefore the term 'build up layer" in the claims is being considered to have an obvious meaning as a "layer of material" or "material structure" in the broadest sense.

Though Jin et al teaches use of filler materials having a negative coefficient of expansion he fails to specifically mention use of zirconium tungstate. Substrates formed with at least one binder and at least one filler having a negative coefficient of expansion are taught by both Starkovich and Chung and where said one filler comprises zirconium tungstate. It would have therefore been obvious to one having ordinary skill in this art to use zirconium tungstate as recited in claims 2, 5 and zirconium tungstate having the characteristics recited in claims 3,6 in the device because the materials suggested by Jin et al are not limited to those in particular and Col. 2, lines 60-65 teach use of negative coefficient of expansion materials having the characteristics recited in claims 3, 6 which would include zirconium tungstate and used of zirconium tungstate as a filler material for the purpose of reducing the coefficient of thermal expansion of the build up layer to closely match that of the chip is also taught by Starkovich and Chuang to be well known.

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jin et al.

Jin et al teaches a method of making an electronic device and provides in figure 7 a substrate 61 having formed of a build up layer comprising at least one binder (i.e.

epoxy) and at least one filler having a negative coefficient of expansion. Die 63 in figure 7 is provided and interconnect 64 is formed and is disposed between the substrate and the die whereby said die is bonded with said interconnect.

The term "build up" layer fails to be specifically defined in the claims fails to have a special meaning that would limit the structure of said layer. Further said term is not established to have any well known meaning in this art to define it to have a specific characteristic. Therefore the term 'build up layer" in the claims is being considered to have an obvious meaning as a "layer of material" or "material structure" in the broadest sense.

Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jin et al in view of Starkovich and Chuang.

The features of Jin et al relative to the claims in which these claims depend have been discussed above. Though Jin et al teaches use of filler materials having a negative coefficient of expansion he fails to specifically mention use of zirconium tungstate. Substrates formed with at least one binder and at least one filler having a negative coefficient of expansion are taught by both Starokvich and Chung and where said one filler comprises zirconium tungstate. It would have therefore been obvious to one having ordinary skill in this art to use zirconium tungstate as recited in claim 23 because the materials suggested by Jin et al are not limited to those in particular and Col. 2, lines 60-65 teach use of negative coefficient of expansion materials having the characteristics would include materials such as zirconium tungstate taught by

Starkovich and Chuang to be well known for the purpose of reducing the coefficient of thermal expansion of the build up layer to closely match that of the chip.

Claims 10, 12, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Papathomas in view of Jin et al.

Papathomas shows in figure 1 an electronic device having a die 6 bonded with a next level package (i.e. substrate 2) and at least one interconnect (i. e. solder balls and pads-not labeled) are shown disposed between the die and the next level package. An underfill 14 in disposed at least in part between the die and the next level package and comprises at least one binder and at least one filler (i.e. zirconium tungstate). Said die is shown bonded to the next level package by said interconnect and underfill.

Col. 2, lines 60-65 of Jin et al teaches use of negative coefficient of expansion filler materials having the characteristics recited in claims 20. It would have been obvious to one having ordinary skill in this art that the zirconium tungstate filler of Papathomas have a isotropic coefficient of thermal expansion of approximately -4.9 ppm/degree C or less because the materials of Jim et al are also used for the purpose of reducing the coefficient of thermal expansion of the build up layer to closely match that of the chip.

With respect to claim 12, the teaching of the underfill of Papathomas as having a low viscosity is deemed to obviously suggest that said underfill may have a no flow characteristic.

With respect to claim 21, the next level package is chosen from a group comprising substrates.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Papathomas in view of Jin et al.

Papathomas teaches and shows in figure 1 a method of bonding a semiconductor die 6 with a next level package (i.e. substrate 2) and also providing at least one interconnect (i. e solder balls and pads-not labeled) is shown disposed at least in part between the die and the next level package. An underfill 14 is also provided at least in part between the die and the next level package and comprises at least one binder and at least one filler (i.e. zirconium tungstate).

Said die is bonded or joined to the next level package by said interconnect and underfill.

Col. 2, lines 60-65 of Jin et al teaches use of negative coefficient of expansion filler materials having the characteristics recited in claims 20. It would have been obvious to one having ordinary skill in this art that the zirconium tungstate filler of Papathomas have a isotropic coefficient of thermal expansion of approximately -4.9 ppm/degree C or less because the materials of Jim et al are also used for the purpose of reducing the coefficient of thermal expansion of the build up layer to closely match that of the chip.

With respect to claim 21, the next level package is chosen from a group comprising substrate

Claims 1-7, 10, 12, 14, 17, 18, 19, 20, 21, 22, 23 are rejected.

PTO-892 cites prior art references that show material with at least one binder and one filler material and use of zirconium tungstate.

Any inquiry concerning this communication should be directed to S. V. Clark at telephone number (571) 272-1725.

S. V. Clark
Primary Examiner
Art Unit 2815

February 6, 2006